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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/029,608	05/15/1998	NORIO FUKASAWA	980233	6285

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/029,608	FUKASAWA ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *109-112,115,116,119,120,123,127 and 129-135* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *109-112,115,116,119,120,123,127 and 129-135* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 109-112, 131, 134 and 135 are rejected under 35 U.S.C. 102(e) as being anticipated by Yasunaga (5656863).

At column 1, line 1 to column 2, line 5, column 2, lines 37-57, column 3, lines 7-47, column 16, line 16 to column 18, line 12, and column 25, lines 44-47, Yasunaga discloses the following:

109. A semiconductor device comprising: a semiconductor element 113 having a surface on which protruding electrodes 112 are formed; a molded resin layer 111 formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof, said end portions protruding a height from the resin layer; and external connection protruding electrodes 53b provided to the end portions of the protruding electrodes that protrude from the resin layer, said external connection protruding electrodes forming a bump, said bump having a height larger than said height of said protruding electrode protruding beyond said resin layer.

110. The semiconductor device as in 109 wherein both a side portion of the resin layer 121 and a side 109, portion of the semiconductor element 125 are respectively exposed.

111. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes having convex end portions are formed; a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except the convex end portions thereof, said convex end portions protruding a height from the resin layer; and external connection protruding electrodes provided to the convex end portions of the protruding electrodes that protrude from the resin layer, said external connection protruding electrodes forming a bump, said bump

having a height larger than said height of said protruding electrode protruding beyond said resin layer.

112. The semiconductor device as in 111, wherein both of a side portion of the resin layer 121 and a side portion of the semiconductor element 125 are respectively exposed.

131. A semiconductor device comprising: a semiconductor element 3 having a surface on which protruding electrodes 9, 10 are formed; a molded resin layer 1 formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof ("top surface of the first conductor 9"); and external connection protruding electrodes 10 provided to the end portions of the protruding electrodes that protrude from the molded resin layer, the molded resin layer and the semiconductor element having surfaces.

Although Yasunaga does not appear to explicitly disclose that the molded resin layer is a compression-molded layer, the product of Yasunaga inherently possesses the structural characteristics imparted by this process limitation. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

Claims 109-112, 131, 134 and 135 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasunaga as applied to claims

109-112, 131, 134 and 135 supra, and further in combination with Kitaura (4956132).

Although Yasunaga does not appear to explicitly disclose that the molded resin layer is compression-molded, as cited, Yasunaga discloses a transfer/injection molded resin layer. Furthermore, at column 1, lines 26-34, Kitaura teaches that a transfer/injection molded resin layer and a compression molded resin layer are equivalents; therefore, it would have been obvious to substitute the compression molded resin layer of Kitaura for the transfer/injection molded resin layer of Yasunaga.

Claims 115, 116, 119 and 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Karnezos (4813129) and Yasunaga (5656863).

At column 5, line 42 to column 7, line 27, Karnezos discloses the following:

115. A semiconductor device comprising: a semiconductor element 12 having a surface on which electrode pads ["contact pads"] connected to an internal part of the semiconductor element and protruding electrodes 16c to be connected to an external part are formed; lead lines 46c each connecting one of the electrode pads ["traces terminating at contact pads"] and one of the protruding electrodes so that the protruding electrodes and the internal pad are connected through the lead lines; and a resin layer 42c formed on

the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof, the protruding electrodes having a core portion 18c and an electrically conductive film 20c formed on a surface of the core portion, the core portions of the protruding electrodes are directly formed on the lead lines, wherein the core portion comprises an elastic resin, a part of said protruding electrode sealed by said resin layer and said end portions are covered commonly with said electrically conductive film.

116. The semiconductor device as in 115: wherein the elastic resin is polyimide.

119. A semiconductor device comprising: a semiconductor element 12 having a surface on which electrode pads ["contact pads"] connected to an internal part of the semiconductor element and protruding electrodes 16c to be connected to an external part are formed; lead lines 46c each connecting one of the electrode pads ["traces terminating at contact pads"] and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and an insulating layer 42c formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof; and external connection protruding electrodes 50c provided to the end portions of the protruding electrodes that protrude from the resin layer, the protruding electrodes

having a core portion 18c and an electrically conductive film 20c formed on a surface of the core portion, the core portions of the protruding electrodes are directly formed on the lead lines, wherein the core portion comprises an elastic resin, and a part of said protruding electrode sealed by said resin layer and said end portions are covered commonly with said electrically conductive film.

120. The semiconductor device as in 119, wherein the elastic resin is polyimide.

To further clarify the disclosure that the electrode pads are connected to an internal part of the semiconductor element and the protruding electrodes and the internal part are connected through the lead lines, it is noted that it is inherent that the semiconductor element comprises an internal part, and the pads, internal part, protruding electrodes, and lead lines are at least physically connected to each other.

To further clarify the disclosure that a part of said protruding electrode sealed by said resin layer and said end portions are covered commonly with said electrically conductive film, is noted that the film lies over commonly the electrode and the layer.

However, Karnezos does not appear to explicitly disclose that the insulating layer 42c is a resin layer.

Notwithstanding, at column 32, lines 27-44, Yasunaga discloses a resin insulating layer 1. In addition, it would have been obvious to combine the product of Yasunaga with the product of Karnezos because it would provide an insulating layer.

Claims 123, 127, 129 and 130 are rejected under 35 U.S.C. 102(b) as being anticipated by Brooks (5824569).

At column 1, lines 20-24, column 2, line 29 to column 4, line 61, and column 5, lines 14-22, Brooks discloses the following:

127. A semiconductor device comprising: a semiconductor element 104 having a surface on which protruding electrodes 130 are formed; and a molded resin layer 110 formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof, wherein the molded resin layer and the semiconductor element have the structure of surfaces defined by cutting using a dicer ["segmented using a saw blade"].

123. A semiconductor device as in 127 wherein a part of a side portion of the semiconductor element being covered with the resin layer, a part of a side portion of said semiconductor element being exposed.

129. The semiconductor device as in 127 wherein a side surface of the resin layer and a side surface of the semiconductor device are flush with each other.

130. The semiconductor device as in 127, wherein end portions of the protruding electrodes protrude from the molded resin layer.

Also, although Brooks does not appear to explicitly disclose that the molded resin layer is compression-molded, the product of Brooks inherently possesses the structural characteristics imparted by this process limitation.

Claims 132 and 133 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks (5824569).

As cited supra, in a first embodiment, Brooks discloses the following:

132. A semiconductor device characterized by comprising: a semiconductor element 30 having protruding electrodes 32 formed on a surface thereof: a first resin layer 36B that is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof; and a second passivation layer 36A provided so as to cover at least a back surface of the semiconductor element, wherein the surface of the semiconductor element is formed with an electronic circuit [32 and "bond pad,"], the first and second resin layers being formed of a molded layer.

133. A semiconductor device as in 132, wherein a sidewall surface of said first passivation layer and a sidewall surface of said second passivation layer form a flush surface with said sidewall surface of said semiconductor element.

However, in the first embodiment, Brooks does not appear to explicitly disclose a sidewall surface of said semiconductor element being exposed at a sidewall surface of said semiconductor device.

Regardless, as cited, in a second embodiment, Brooks discloses a sidewall surface of a semiconductor element 104 being exposed at a sidewall surface of the semiconductor device. In addition, it would have been obvious to combine the second embodiment of Brooks with the first embodiment because it would enable simultaneous processing of multiple devices.

Also, although Brooks does not appear to explicitly disclose the first and second molded layers being formed of a compression molded layer, the product of Brooks inherently possesses the structural characteristics imparted by this process limitation.

Claims 123, 127, 129, 130, 132 and 133 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks as applied to claims 123, 127, 129, 130, 132 and 133 supra, and further in combination with Kitaura (4956132).

Although Brooks does not appear to explicitly disclose that the molded resin layer is compression-molded, as cited, Brooks discloses a casting molded "gravity leveling" resin layer. Furthermore, at column 1, lines 26-34, Kitaura teaches that a casting molded resin layer and a compression

molded resin layer are equivalents; therefore, it would have been obvious to substitute the compression molded resin layer of Kitaura for the casting molded resin layer of Brooks.

Applicant's amendment and remarks filed 12-19-3 have been fully considered, are addressed in the rejection supra, and are further addressed infra.

Applicant asserts that the applied prior art does not disclose the claimed compression-molding process limitations and the compression-molded resin layer.

This assertion is respectfully deemed to be unpersuasive because the applied prior art is not relied on in the rejection for a disclosure of a compression-molding process. Moreover, it is noted that rejection under 35 U.S.C. 102 and/or 35 U.S.C. 103 is indicated where prior art discloses a product that appears to be either identical with or only slightly different from the product claimed in a product by process claim. Further, applicant can be required, to prove that the prior art product does not necessarily or inherently possess characteristics of the claimed product. Whether the rejection is based on inherency under 35 U.S.C. 102, on prima facie obviousness under 35 U.S.C. 103, jointly or alternatively, the burden of proof is the same. When, as here, there is reason to believe that the functional limitation asserted to be critical for establishing novelty in the

claimed subject matter is an inherent characteristic of the prior art, the Office possesses authority to require applicant to prove that subject matter shown to be in the prior art does not possess the characteristic relied on. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

Relatedly, applicant compares the alleged claimed molding process and molded resin with another molding process and molded resin. However, this comparison is respectfully deemed unpersuasive because applicant provides no evidence that the claims are limited to the alleged claimed molding process and resin, or that the applied prior art discloses the alleged other molding process and resin.

Also, applicant contends that, "Karnezos fails to teach the claimed common electrically conductive film since the Examiner relies upon a teaching both a film 50c and a film 46c, which clearly are not the same film."

This contention is respectfully deemed unpersuasive because the claims are not limited to a common electrically conductive film, and the prior art is not necessarily applied to the rejection for this disclosure.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 12-19-3 prompted the new grounds of rejection over Kitaura presented in this Office

action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 571-272-2815.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
10-Mar-04